EAT315124 – ELECTRONICS AND ADVANCED TECHNOLOGIES

EXTERNAL EXAM INFORMATION SHEET

Basic Formulae

Ohm's law $V = IR, I = \frac{V}{R}, R = \frac{V}{I}$	**Watt's law** $P = VI, P = I^2R, P = \frac{V^2}{R}$
Series resistors $R_T = R_1 + R_2 + \cdots$	**Parallel resistors** $R_T = \left({R_1}^{-1} + {R_2}^{-1} + \cdots\right)^{-1}$ **or** $\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots$
Parallel capacitors $C_T = C_1 + C_2 + \cdots$	**Series capacitors** $C_T = \left({C_1}^{-1} + {C_2}^{-1} + \cdots\right)^{-1}$ **or** $\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots$
RC time constant $T_c = RC$	**Frequency, period** $f = \frac{1}{T}$
Transistor DC current gain (hFE, β) $\beta = \frac{I_{Collector}}{I_{Base}}$	**Voltage divider** $V_{out} = V_{in} \times \frac{R_{out}}{R_{Total}}$
Voltage gain $G = \frac{V_{out}}{V_{in}}$ Inverting op-amp: $G = \frac{-R_f}{R_i}$ Non-inverting op-amp: $G = 1 + \frac{R_f}{R_i} = \frac{R_f + R_i}{R_i}$ Class A: $G \approx \beta$ Class B: $G = 1$	
AC voltage $V_{peak} = \frac{1}{2}V_{peak-peak} = 1.414V_{RMS}$ $V_{RMS} = 0.707V_{peak}$	

TASMANIAN ASSESSMENT, STANDARDS & CERTIFICATION

Prefixes

Prefix	Symbol	Factor	Power
giga	G	1000000000	10^{9}
mega	M	1000000	10^{6}
kilo	k	1000	10^{3}
(none)	(none)	1	10^{0}
milli	m	0.001	10^{-3}
micro	μ	0.000001	10^{-6}
nano	n	0.000000001	10^{-9}
pico	p	0.000000000001	10^{-12}

Resistor colour code

Colour	Digit	Multiplier	Tolerance
Silver		×0.01	±10%
Gold		×0.1	±5%
Black	0	×1	
Brown	1	×10	±1%
Red	2	×100	±2%
Orange	3	×1000	±0.05%
Yellow	4	×10000	±0.02%
Green	5	×100000	±0.5%
Blue	6	×1000000	±0.25%
Violet	7		±0.1%
Gray	8		±0.01%
White	9		

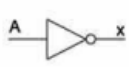
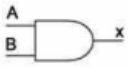
E12 series:

10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82

pF code:

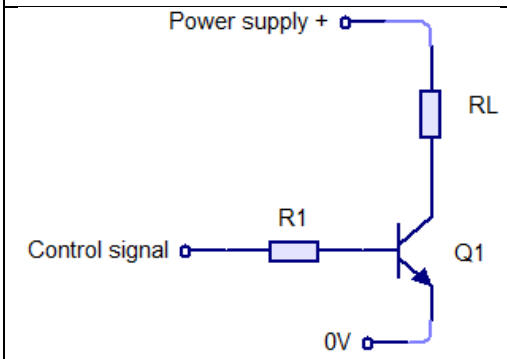
First two numerals represent first two digits of value in picofarads. Third numeral represents multiplier (power pf 10).

Logic gates: Boolean, Symbols, Truth tables

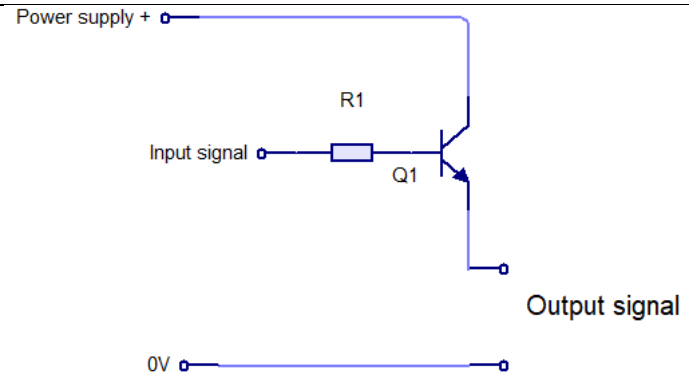
Name	NOT	AND	NAND	OR	NOR	XOR	XNOR
Alg. Expr.	$\overline{A}$	AB	$\overline{AB}$	$A+B$	$\overline{A+B}$	$A \oplus B$	$\overline{A \oplus B}$
Symbol							
Truth Table	A X 0 1 1 0	B A X 0 0 0 0 1 0 1 0 0 1 1 1	B A X 0 0 1 0 1 1 1 0 1 1 1 0	B A X 0 0 0 0 1 1 1 0 1 1 1 1	B A X 0 0 1 0 1 0 1 0 0 1 1 0	B A X 0 0 0 0 1 1 1 0 1 1 1 0	B A X 0 0 1 0 1 0 1 0 0 1 1 1

Single NPN Transistor Topologies

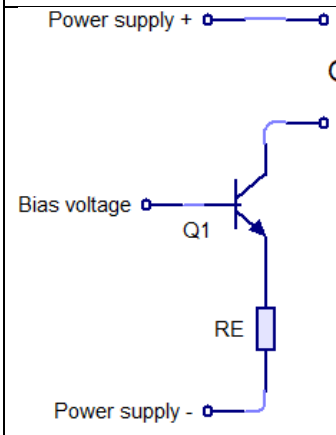
Common emitter



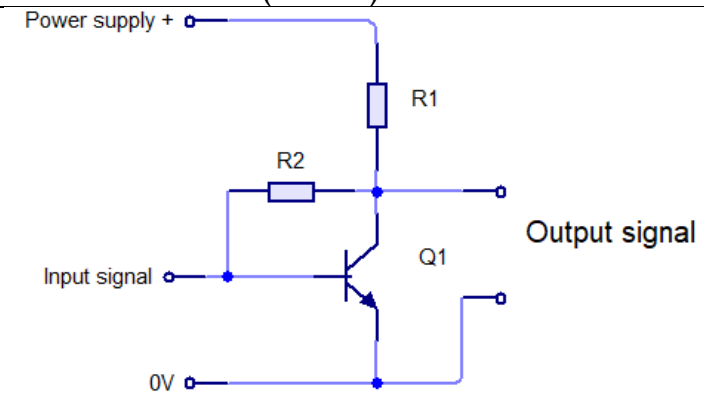
Common collector



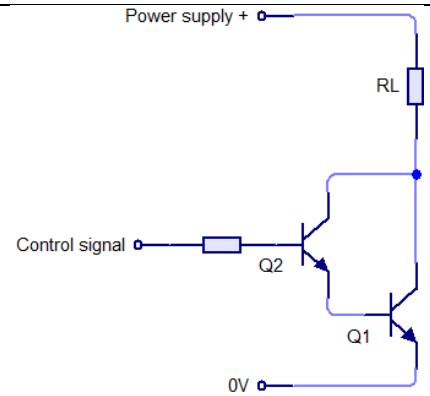
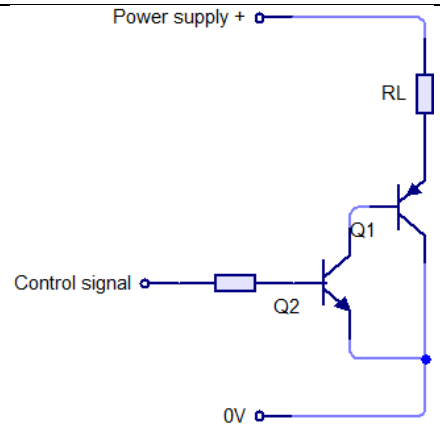
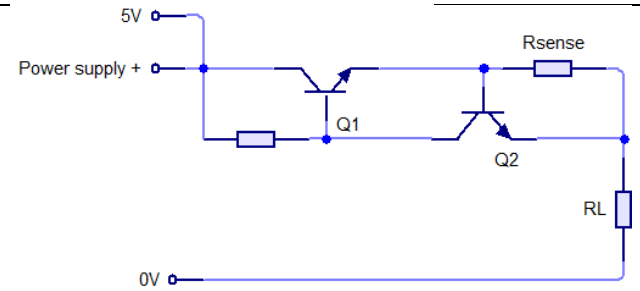
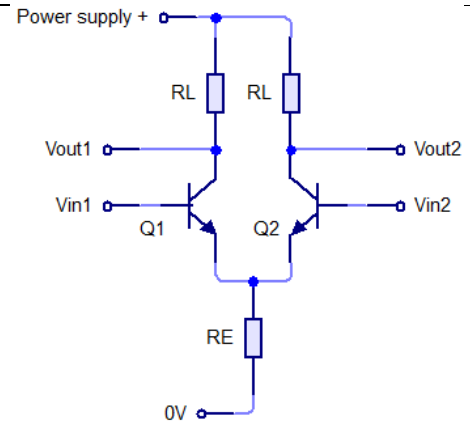
Common base

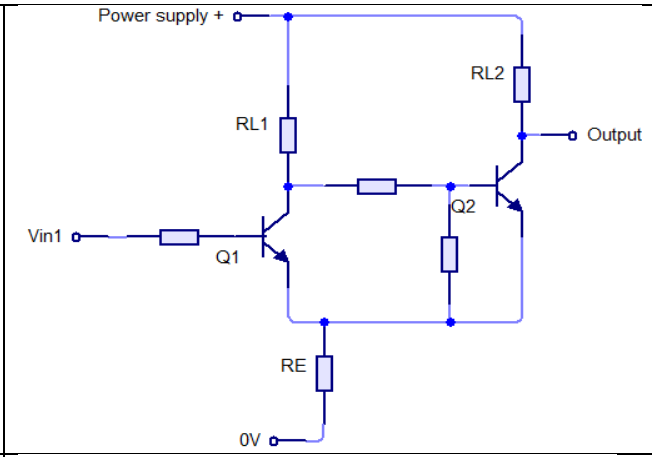
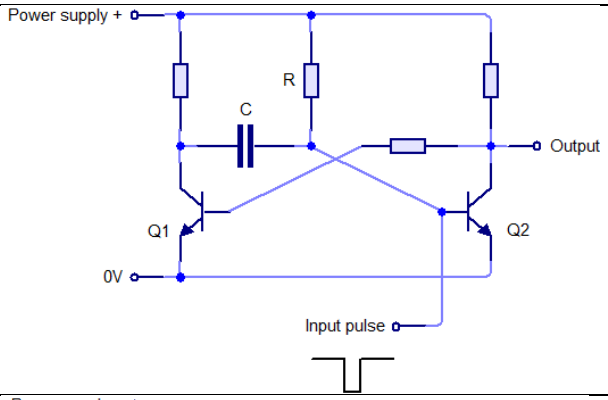
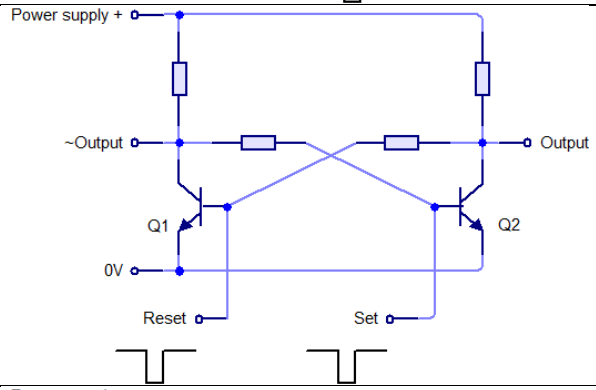
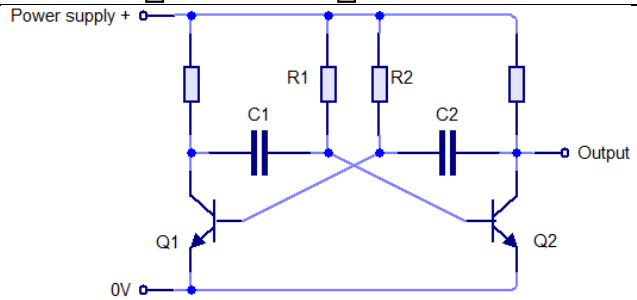


Collector feedback (Class A)



Transistor blocks

Darlington $\beta_T = \beta_{Q1} \times \beta_{Q2}$	
Sziklai $\beta_T = \beta_{Q1} \times \beta_{Q2}$	
Current limiting $V_{Rsense} \approx 0.7V$	
Differential Pair (long tail) $V_{out1} - V_{out2} = -\beta \times (V_{in1} - V_{in2})$	

Schmitt Trigger Low switching threshold: $V_L \approx V_+ \times \frac{R_E}{R_E+R_{L1}}$ High switching threshold: $V_H \approx V_+ \times \frac{R_E}{R_E+R_{L2}}$	
Monostable Output pulse time $T \approx 0.69RC$	
Bistable	
Astable (Relaxation Oscillator) Period: $T \approx 0.69R_1C_1 + 0.69R_2C_2$	
Push-pull output stage (Class B)